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EXAMINER	
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ART UNIT	PAPER NUMBER
2615	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/707,815	KATOH, SATOSHI	
	Examiner	Art Unit	
	Gevell Selby	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-22* is/are allowed.

6)☒ Claim(s) *1,4-10 and 13-18* is/are rejected.

7)☒ Claim(s) *2,3,11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 November 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 4, 5, 8, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keiji, JP 09-093470 in view of Hidekage, JP 08-125924 and Azim, US 6,137,533.

In regard to claim 1, Keiji discloses an image taking apparatus, comprising:

a solid state image taking device (see figure 1, element 12) which converts an optical image of a subject to be taken to analog video signals and outputs said analog video signals (see paragraph 11);

an analog to digital (A/D) converter (see figure 1, element 16) which converts at a designated quantization bit number said analog video signals outputted from said solid state image taking device to digital video signals having said designated quantization bit number (see paragraph 13: It is implied that the

A/D converter has a designated quantization bit number to covert the quantized analog sample into a digital signal.);

a digital signal processor (see figure 1, element 21) which generates a designated signal processing bit number that is used in an image process applied to said digital video signals outputted from said A/D converter (see paragraph 16: It is implied that the DSP will have a designated bit number in order to be able to read in the signal from the A/D converter);

a displaying apparatus (see figure 1, element 36) which displays said digital video signals outputted from said DSP (see paragraph 18); and

a recording medium (see figure 1, element 23) which stores said digital video signals outputted from said DSP (see paragraph 17).

The Keiji reference does not disclose comprising:

a system controller that generates a bit number converting signal;

the digital signal processor receiving said bit number converting signal; and wherein said designated quantization bit number and said designated signal processing bit number at said A/D converter are variable.

Hidekage, JP 08-125924, discloses as solid state image pickup device and line sensor camera with an A/D converter (108) has a number-of-bits selection means that selects N bits where if N >= M, M bits are used and if N < M, N bits are used (see paragraphs 12 and 29). The system controller detects the condition of the number-of-bits selection means and the number-of-bits of the A/D converter. Hidekage, JP 08-125924

teaches that large numbers of bits are needed for photography of the large photographic subject of a dynamic range but the system will become expensive (see paragraph 11).

It would have been obvious to a person skilled in the art at the time of invention to have been motivated to modify Keiji, JP 09-093470 in view of Hidekage, JP 08-125924, to have an A/D converter with a number-of-bits selection means to change the quantization bit number and a system controller that stores the quantization bit number of the A/D converter in order to extend the dynamic range that can be photographed as taught by Hidekage, JP 08-125924.

Azim, US 6,137,533, discloses an image capturing device with a digital signal processor that receives a digital video signal from the A/D converter that can either have a quantization bit number of 12 bits, when a digital gain is applied, or 10 bits (see column 6, lines 23-26 and column 8, lines 4-7). When the bit number is 12 bits, a compander inside the DSP can be used to compress the signal back into 10 bits as in the A/D converter (see column 6, lines 26-28 and column 8, lines 20-22).

It would have been obvious to a person skilled in the art at the time of invention to have been motivated to modify Keiji, JP 09-093470 in view of Hidekage, JP 08-12592, and in view of Azim, US 6,137,533, to have said signal processing bit number at said DSP be variable, and said signal processor receives the bit number stored in the system controller in order to process the same number of bits as sent from the A/D converter to provide increased dynamic range without loosing image information.

In regard to claim 4, Keiji, JP 09-093470 in view of Hidekage, JP 08-125924, and in view of Azim, US 6,137,533, discloses an image taking apparatus in accordance with claim 1, but lacks wherein:

said signal processing bit number at said DSP is variable, and said signal processing bit number is made to be the same bit number of said quantization bit number at said A/D converter, when said digital video signals are displayed on said displaying apparatus (see Azim: column 6, lines 26-28 and column 8, lines 20-22: a compander inside the DSP can be used to compress the signal back into the same number of bits as in the A/D converter).

In regard to claim 5, Keiji, JP 09-093470 in view of Hidekage, JP 08-125924, and in view of Azim, US 6,137,533, discloses an image taking apparatus in accordance with claim 1, further comprising:

a mode setting switch (circuit changing switch) for setting an operation mode at said image taking apparatus (see Keiji: paragraph 20),

wherein said system controller (see Hidekage: figure 1, element 105) generates said bit number converting signal for setting said quantization bit number at said A/D converter and said signal processing bit number at said DSP based on said operation mode set at said mode setting switch, and outputs said bit number converting signal to said A/D converter and said DSP (see Hidekage: paragraphs 14, 21-24, and 29; If N >= M, the controller selects M bits and if N < M, N bits are used.), wherein:

said A/D converter sets said quantization bit number based on said bit number converting signal outputted from said system controller (see Hidekage: paragraphs 21 and 23).

In regard to claim 8, Keiji, JP 09-093470 in view of Hidekage, JP 08-125924, and in view of Azim, US 6,137,533, as described in regard to claim 1, discloses an image taking apparatus in accordance with claim 1, further comprising

a displaying apparatus driver for making said digital video signals display on said displaying apparatus by thinning out a part of said digital video signals outputted from said DSP (see Keiji: paragraph 22).

In regard to claim 9, Keiji, JP 09-093470 in view of Hidekage, JP 08-125924, and in view of Azim, US 6,137,533, as described in regard to claim 1, discloses an image taking apparatus in accordance with claim 1, wherein

said image taking apparatus is an electronic still camera (see Keiji: paragraph 9 and figure 1, element SV).

2. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keiji, JP 09-093470 in view of Hidekage, JP 08-125924, and in view of Azim, US 6,137,533, as applied to claim 1 above, and further in view of Lee, US 5,301,026.

In regard to claim 6, Keiji, JP 09-093470 in view of Hidekage, JP 08-125924, and in view of Azim, US 6,137,533, discloses an image taking apparatus in accordance with claim 5. The Keiji, Hidekage, and Azim references do not disclose wherein

said system controller, in case that said digital video signals stored in said recording medium are displayed on said displaying apparatus, stops operation of said solid state image taking device, said A/D converter, and said DSP.

Lee, US 5,301,026, discloses a picture editing apparatus in a digital still video camera system that has a read-out mode the user can select with an input key to view images saved in the memory card and the system controller displays the image on the display(see column 4, line 60 to column 5, lines 11). When the modes are switched from image capture mode to read-out mode, it is implied that the system controller stops the operations of the components used in image capture mode until the camera returns to that mode, and begins the operations of the components of the read-out mode because the imager, A/D converter and DSP are not used in reproduction mode (see column 2, lines 50-62).

It would have been obvious to a person skilled in the art at the time of invention to have been motivated to modify Keiji, JP 09-093470 in view of Hidekage, JP 08-125924, as applied to claim 1 above, further in view of Azim, US 6,137,533, as applied to claim 4 above, and further in view of Lee, US 5,301,026, to have a read-out mode wherein:

the system controller stops operation of said solid state image taking device, said A/D converter, and said DSP, in order to view images from memory on the display as taught by Lee.

In regard to claim 7, Keiji, JP 09-093470 in view of Hidekage, JP 08-125924, and in view of Azim, US 6,137,533, and further in view of Lee, US 5,301,026, discloses an image taking apparatus in accordance with claim 5, wherein

said mode setting switch (circuit changing switch), in case that said digital video signals have been stored in said recording medium, selects whether said digital video signals stored in said recording medium are made to display on said displaying apparatus or not (see Keiji: paragraph 20).

3. Claims 10, 13, 14, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keiji, JP 09-093470, in view of Hidekage, JP 08-12592, Azim, US 6,137,533, and Nishikawa, 4,566,074.

In regard to claim 10, Keiji, JP 09-093470, discloses an image taking apparatus, comprising:

a solid state image taking device (see figure 1, element 12) which converts an optical image of a subject to be taken to analog video signals and outputs said analog video signals (see paragraph 11);

an analog to digital (A/D) converter (see figure 1, element 16) which converts at a designated quantization bit number said analog video signals outputted from said solid state image taking device to digital video signals having said designated quantization bit number (see paragraph 13: It is implied that the A/D converter has a designated quantization bit number covert the quantized analog sample into a digital signal);

a digital signal processor (see figure 1, element 21) which applies an image process to said digital video signals outputted from said A/D converter at a designated signal processing bit number (see paragraph 16: It is implied the DSP will have a designated bit number in order to be able to read in the signal from the A/D converter);

a displaying apparatus (see figure 1, element 36) which displays said digital video signals outputted from said DSP (see paragraph 18); and

a recording medium (see figure 1, element 23) which stores said digital video signals outputted from said DSP (see paragraph 17).

The Keiji reference does not disclose comprising:

a system controller that generates a bit number converting signal;

the digital signal processor receiving said bit number converting signal;

wherein said A/D converter provides plural A/D converting sections in which the quantization bit number of each of said plural A/D converting sections is different between them and is fixed, and either one of said plural A/D converting sections converts said analog video signals outputted from said solid state image taking device to digital video signals, and outputs said digital video signals to said DSP;

and wherein said signal processing bit number is variable.

Hidekage, JP 08-125924, discloses a system controller (105) that detects the condition of the number-of-bits selection means and the number-of-bits of the A/D converter (see paragraph 21). Hidekage, JP 08-125924 teaches that large numbers of bits

are needed for photography of the large photographic subject of a dynamic range but the system will become expensive (see paragraph 11).

It would have been obvious to a person skilled in the art at the time of invention to have been motivated to modify Keiji, JP 09-093470 in view of Hidekage, JP 08-125924, to have a system controller that stores the quantization bit number of the A/D converter in order to extend the dynamic range that can be photographed as taught by Hidekage, JP 08-125924.

Azim, US 6,137,533, discloses an image capturing device with a digital signal processor that receives a digital video signal from the A/D converter that can either have a quantization bit number of 12 bits, when a digital gain is applied, or 10 bits (see column 6, lines 23-26 and column 8, lines 4-7). When the bit number is 12 bits, a compander inside the DSP can be used to compress the signal back into 10 bits as in the A/D converter (see column 6, lines 26-28 and column 8, lines 20-22).

It would have been obvious to a person skilled in the art at the time of invention to have been motivated to modify Keiji, JP 09-093470 in view of Hidekage, JP 08-12592, and in view of Azim, US 6,137,533, to have said signal processing bit number at said DSP be variable, and said signal processor receives the bit number stored in the system controller in order to process the same number of bits as sent from the A/D converter to provide increased dynamic range without loosing image information.

Nishikawa, US 4,566,074, discloses and image taking apparatus with two A/D converters having the same number of bits or with one converter being set higher than the other depending on the mode of use (see column 11, lines 39-42) so that the smallest

number of quantizing bits can be used whenever possible to save power (see column 2, lines 36-39).

It would have been obvious to a person skilled in the art at the time of invention to have been motivated to modify Keiji, JP 09-093470, in view of Hidekage, JP 08-12592, Azim, US 6,137,533, and Nishikawa, 4,566,074, to have two A/D converting sections in which the quantization bit number of each of said plural A/D converting sections is different between them and is fixed, and either one of said plural A/D converting sections converts said analog video signals outputted from said solid state image taking device to digital video signals, and outputs said digital video signals to said DSP in order to use the smaller A/D converter that saves power, when a large quantization bit number is not required, as taught by Nishikawa.

In regard to claim 13, Keiji, JP 09-093470, in view of Hidekage, JP 08-12592, Azim, US 6,137,533, and Nishikawa, 4,566,074, discloses an image taking apparatus in accordance with claim 10, but lacks wherein said signal processing bit number is made to be the same bit number of said quantization bit number at said A/D converter, in case that said digital video signals are displayed on said displaying apparatus (see Azim: column 6, lines 26-28 and column 8, lines 20-22: a compander inside the DSP can be used to compress the signal back into the same number of bits as in the A/D converter).

In regard to claim 14, Keiji, JP 09-093470, in view of Hidekage, JP 08-12592, Azim, US 6,137,533, and Nishikawa, 4,566,074, discloses an image taking apparatus in accordance with claim 10, further comprising:

a mode setting switch (circuit changing switch) for setting an operation mode at said image taking apparatus (see Keiji: paragraph 20); and

a system controller (see Azim: figure 1, element 110) which generates a bit number converting signal for setting said quantization bit number at said A/D converter and said signal processing bit number at said DSP (see Azim: column 8, lines 10-22) based on said operation mode set at said mode setting switch, and outputs said bit number converting signal to said A/D converter and said DSP (see Nishikawa: column 11, lines 39-42),

[By using the multiple A/D converters of the Nishikawa reference with varying quantization bit numbers, it would have been obvious and expected that the system controller of Azim would output the bit number converting signal to the correct A/D converting section based on the mode.] wherein:

said switching circuit selects either one of said plural A/D converting sections based on said A/D converting section changing signal outputted from said system controller (see Keiji: paragraph 20); and

said DSP sets said signal processing bit number based on said bit number converting signal outputted from said system controller (see Azim: column 8, lines 20-22; It is implied the system controller sends a signal to the DSP whether or not to use the compander).

In regard to claim 17, Keiji, JP 09-093470, in view of Hidekage, JP 08-12592, Azim, US 6,137,533, and Nishikawa, 4,566,074, discloses an image taking apparatus in accordance with claim 10, further comprising:

a displaying apparatus driver for making said digital video signals display on said displaying apparatus by thinning out a part of said digital video signals outputted from said DSP (see Keiji: paragraph 22).

In regard to claim 18, Keiji, JP 09-093470, in view of Hidekage, JP 08-12592, Azim, US 6,137,533, and Nishikawa, 4,566,074, discloses an image taking apparatus in accordance with claim 10, wherein:

said image taking apparatus is an electronic still camera (see Keiji: paragraph 9 and figure 1, element SV).

4. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keiji, JP 09-093470, in view of Hidekage, JP 08-12592, Azim, US 6,137,533, and Nishikawa, 4,566,074, as applied to claim 10 above, and further in view of Lee, US 5,301,026.

In regard to claim 15, Keiji, JP 09-093470, in view of Hidekage, JP 08-12592, Azim, US 6,137,533, and Nishikawa, 4,566,074, discloses an image taking apparatus in accordance with claim 14, but lacks that wherein:

said system controller, in case that said digital video signals stored in said recording medium are displayed on said displaying apparatus, stops operation of said solid state image taking device, said A/D converter, and said DSP.

Lee, US 5,301,026, discloses a picture editing apparatus in a digital still video camera system that has a read-out mode the user can select with an input key to view images saved in the memory card and the system controller displays the image on the display(see column 4, line 60 to column 5, lines 11). When the modes are switched from image capture mode to read-out mode, it is implied that the system controller stops the

operations of the components used in image capture mode until the camera returns to that mode, and begins the operations of the components of the read-out mode because the imager, A/D converter and DSP are not used in reproduction mode (see column 2, lines 50-62).

It would have been obvious to a person skilled in the art at the time of invention to have been motivated to modify Keiji, JP 09-093470, in view of Hidekage, JP 08-12592, Azim, US 6,137,533, and Nishikawa, 4,566,074, and further in view of Lee, US 5,301,026, to have a read-out mode wherein:

the system controller stops operation of said solid state image taking device, said A/D converter, and said DSP, in order to view images from memory on the display as taught by Lee.

In regard to claim 16, Keiji, JP 09-093470, in view of Hidekage, JP 08-12592, Azim, US 6,137,533, and Nishikawa, 4,566,074, and further in view of Lee, US 5,301,026, discloses an image taking apparatus in accordance with claim 14, wherein:

said mode setting switch (circuit changing switch), in case that said digital video signals have been stored in said recording medium, selects whether said digital video signals stored in said recording medium are made to display on said displaying apparatus or not (see Keiji: paragraph 20).

Allowable Subject Matter

3. Claims 19-22 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art taken alone or in combination lacks the limitation the A/D converter makes the quantization bit number in the case that the digital video signals are displayed on the displaying apparatus smaller than the quantization bit number when the digital video signals are stored in the recording medium as claimed in claims 19 and 21 or transferred to an external apparatus through the I/F circuit as claimed in claims 20 and 22.

5. Claims 2, 3, 11, and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art taken alone or in combination lacks the limitation the A/D converter makes the quantization bit number in the case that the digital video signals are displayed on the displaying apparatus smaller than the quantization bit number when the digital video signals are stored in the recording medium as claimed in claims 2 and 11 or transferred to an external apparatus through the I/F circuit as claimed in claims 3 and 12; therefore, the claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gevell Selby whose telephone number is 703-305-8623. The examiner can normally be reached on 8:00 A.M. - 5:30 PM (every other Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Christensen can be reached on 703-308-9644. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gvs

TUAN HO
PRIMARY EXAMINER